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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/610,497	06/30/2003	James Stuart Wight	CMA-0009	5376

22832 7590 01/10/2006

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/610,497	WIGHT ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 14-41* is/are pending in the application.

4a) Of the above claim(s) *14-41* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment and RCE filed December 30, 2005. Claims were canceled. Claims 1-2,14-41 are pending, in which claims 14-41 have been newly added.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Election/Restrictions

1. Newly submitted claims 14-41 are directed to an invention that are species and distinct from the invention originally claimed in original claims 1-2 for the following reasons:

a) Group I, originally claimed claims 1-2, is directed to a claimed invention of an integrated circuit package which includes a housing containing an integrated circuit die having at least one circuit etched thereon, the circuit comprising elements which require theoretically negative reactive component values, wherein the die coupled to the housing; and

b) Group II, newly added claims14-41, is directed to a claimed invention of an apparatus, which apparatus at least comprises a first inductor, a second inductor coupled to the first inductor in shunt arrangement, and a third inductor coupled to the first inductor at a second node in a shunt arrangement.

Since applicant has received an action on the merits for the originally presented invention of subject matter of Group I, claims 1-2, this invention Group I, claims 1-2, has been constructively elected by original presentation and examination for prosecution on the merits. There is no generic claim.

2. Accordingly, Group II, new Claims 14-41, is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

3. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Busking et al (6,107,684) in view of Gonda (4,924,195) and Seshita (6,366,770).

Busking et al teach an integrated circuit package comprising an integrated circuit die 5 (Figs 2-4; col 2, line 53 through col 4) having at least one circuit etched thereon (col 1, lines 15-

33), wherein the circuit comprises elements which require theoretical values, and wherein the circuit also includes a on-die component 8 of bond wires (Fig 3B; col 3, lines 20-35); and a housing 11 containing said integrated circuit die 5 (col 2, lines 53-67; col 3, lines 1-14), wherein the integrated circuit die 5 is electrically coupled to the housing using at least one wire bonds 4,6,8 (Figs 1A-4B); and wherein the at least wire bonds have an inductance associated therewith (col 3, lines 50-60; line 28 through col 4; Figs 5,1A-4B), wherein the theoretical values of the elements of the circuit required by the integrated circuit are actually incorporated into the circuit through the use of wire bonds having a pre-determined inductance values, and wherein the wire bond inductance is used to facilitate operation of the at least one circuit as the wire bonds are electrically coupled to the circuits formed in the die and generate an amount of inductance during operation. Busking also discloses a method comprising of making available wire bonds 4,6,8 for electrically connected to circuit formed in the die 5, wherein the wire bonds 4,6,8 generate an amount of inductance during operation of the circuits, so that inductance of the wire bonds are used to facilitate operation of a circuit contained in an integrated circuit package comprising making available wire bond inductance to the circuit from the wire bonds (Figs 5, 1A-4A, col 3, line 15 through col 4), wherein the circuit is contained in an integrated circuit die 5 housed in the integrated circuit package (Figs 1A-4B, col 2, line 53 through col 3).

Busking already teaches an integrated circuit die having at least one circuit including at least one elements 8, but lacks having the circuit comprising an impedance inverter (claim 2) having elements which require theoretically negative reactive component values (claim 1)

However, Gonda teaches (at col 3, lines 9-38) forming an integrated circuit die having at least one circuit, wherein the circuit comprising an impedance inverter (re claim 2, col 3, lines 9-20) which is having elements including negative inductance shunt arms, which elements require theoretically negative reactive component values (re claim 1). Seshita teaches (at Figs 1A,2; col 5, line 16 through col 6) forming an integrated circuit die having at least one circuit, wherein the circuit comprising inductor elements (MC1b, MC2b, MC3b) having theoretical values, wherein the theoretical values of the elements of the circuit required by the integrated circuit are actually incorporated into the circuit through the use of wire bonds 20h,20i,20j having a pre-determined inductance values, and wherein the wire bond inductance is used to facilitate operation of the at least one circuit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit die having at least one circuit of Busking by forming at least one circuit comprising an impedance inverter, which is having elements which require theoretically negative reactive component values, as taught by Gonda and Seshita. This is because of the desirability to form an integrated circuit die of crystal oscillators that can be operated in the high frequency (HF) and ultra high frequency (UHF) band, and to serve as a buffer and impedance transformer between the low impedance output and the high impedance of a load, wherein using available wire bonds as an inductor element would save area for other devices, would reduce processing steps and production cost.

Response to Arguments

4. Applicant's remarks filed December 30, 2005 have been fully considered but they are not persuasive.

Applicant remarked that "...none of the cited documents teaches or discloses that 'negative reactive component values are actually incorporated into the circuit through the use of wire bonds'...".

In response, this is noted and found unconvincing. The rejection is not overcome by pointing out that one reference does not contain a particular limitation when reliance for that teaching is on another reference. In Re Lyons 150 USPQ 741 (CCPA 1966). Moreover, as here, the rejection is based on combinations of references. In Re Keller, 208 USPQ 871 (CCPA 1981); In Re Young, 159 USPQ 725 (CCPA 1968).

As already of record, Gonda (4,924,195) clearly teaches (at col 3, lines 9-20) forming the circuit comprising an impedance inverter which is having elements including ***negative inductance shunt arms, which elements require theoretically negative reactive component values.*** Seshita (6,366,770) teaches (at Figs 1A,2; col 5, line 16 through col 6) forming an integrated circuit die having at least one circuit, wherein the circuit comprising inductor elements (MC1b, MC2b, MC3b) having theoretical values, wherein ***the theoretical values*** of the elements of the circuit required by the integrated circuit ***are actually incorporated into the circuit through the use of wire bonds 20h,20i,20j*** having a pre-determined inductance values, ***and wherein the wire bond inductance is used to facilitate operation of the circuit.***

In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be

some logical reason why skilled in the art would be motivated to make the proposed combination of references. In re Regel 188 USPQ 136 (CCPA 1975). The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin 170 USPQ 209 (CCPA 1971): In Re Rosselet 146 USPQ 183 (CCPA 196). References are evaluated by what they collectively suggest to one versed in the art, rather than by their specific disclosures. In Re Simon, 174 USPQ 114 (CCPA 1972); In Re Richman 165 USPQ 509, 514 (CCPA 1970).

Applicant's apparently argument that the applicant has different reason for, or advantage resulting from doing what the prior art relied upon has suggested, it is noted that it is well settled that this is not demonstrative of non-obviousness, In Re Kronig 190 USPQ 425, 428 (CCPA 1976); In Re Lintner 173 USPQ 560 (CCPA 1972); the prior art motivation or advantage may be different than that of applicant while still supporting a conclusion of obviousness. In Re Wiseman 201 USPQ 658 (CCPA 1979); Ex Parte Obiaya 227 USPQ 58 (Bd. of App. 1985).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oacs-3

Michael Trinh
Primary Examiner